Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (currently amended). A digital system comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases, wherein the microprocessor comprises:

program fetch circuitry operable to perform a first portion of the plurality of pipeline phases;

instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases; and

at least a first functional unit connected to receive control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases, wherein the first functional unit comprises:

byte intermingling circuitry connected to receive a first source operand having an ordered plurality of fields and a second source operand having an ordered plurality of fields and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable, responsive to one of a plurality of byte intermingling instructions, to ~~treat the first and second operands each as a number N1 of ordered fields, such that the~~ place non-contiguous data from selected fields of the first source operand in a most significant portion of the destination operand, and to place non-contiguous data from selected fields of the second source operand that are at the same positions as the selected fields from the first source operand, in a least significant portion of the destination operand ~~consists of a number N2 of fields selected from the N1 fields of the first source operand intermingled with a number N3 of fields selected from the N1 fields of the second source operand; and wherein the first functional unit is operable to provide the~~

~~destination operand intermingled in accordance to each of a set of byte intermingling instructions~~.

2 (original). The digital system of Claim 1, wherein the byte intermingling circuitry is operable to receive the first source operand and second operand and to provide the destination operand during a single pipeline execution phase.

3 (canceled).

4 (canceled).

5 (canceled).

6 (canceled).

7 (currently amended). A ~~The~~ digital system ~~of Claim 6~~, comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases, wherein the microprocessor comprises:

program fetch circuitry operable to perform a first portion of the plurality of pipeline phases;

instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases; and

at least a first functional unit connected to receive control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases, wherein the first functional unit comprises:

byte intermingling circuitry connected to receive a first source operand having an ordered plurality of fields and a second source operand having an ordered plurality of fields and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable, responsive to one of a plurality of byte intermingling instructions, to ~~operable to provide the destination operand by placing~~ place

the contents of a least significant plurality of ~~set of the N1~~ fields selected from the second source operand in a least significant portion of the destination operand and ~~by placing a least~~ to place the contents of a most significant ~~set of the N1~~ plurality of fields selected from the ~~second~~ first source operand in a most significant portion of the destination operand~~, whereby a byte pack operation is performed~~.

8 (canceled).

9 (original). The digital system of Claim 1, further comprising a register file connected to the first functional unit for providing the first and second source operands and connected to the first functional unit to receive the destination operand.

10 (original). The digital system of Claim 1, wherein each of the set of byte intermingling instructions has a field for identifying a predicate register.

11 (currently amended). The digital system of Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the ~~CPU~~ microprocessor via a keyboard adapter;

a display, connected to the ~~CPU~~ microprocessor via a display adapter;

radio frequency (RF) circuitry connected to the ~~CPU~~ microprocessor; and

an aerial connected to the RF circuitry.

12 (currently amended). A method of operating a digital system having a microprocessor and a set of byte intermingling instruction, comprising the steps of:

fetching a ~~first type of~~ byte intermingling instruction for execution;

fetching a first source operand and a second operand selected by the ~~first type of~~ byte intermingling instruction, each of the first and second source operands comprising an ordered plurality of fields; and

~~treating the first and second source operands as a set of N1 fields;~~

writing, into a most significant portion of a destination operand, ~~intermingling~~ non-contiguous data from selected ones of the plurality of ~~N1~~ fields from the first source

operand and writing, into a least significant portion of the destination operand, non-contiguous data from selected ones of the plurality of ~~N1~~ fields from the second source operand that are at the same positions as the selected fields of the first source operand, ~~in a first selected order~~ the data being selected in accordance with the ~~first type of~~ byte intermingling instruction ~~to form a first type of intermingled fields; and writing a destination operand with the first type of intermingled fields~~.

13 (canceled).

14 (currently amended). The method of Claim ~~11~~ 12, wherein the step of ~~intermingling~~ writing is performed during a single execution phase of the microprocessor.

15 (new). The method of Claim 12, wherein the writing step writes most significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand and writes most significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand.

16 (new). The method of Claim 12, wherein the writing step writes least significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand and writes least significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand.

17 (new). A method of operating a digital system having a microprocessor and a set of byte intermingling instruction, comprising the steps of:

fetching a byte intermingling instruction for execution;

fetching a first source operand and a second operand selected by the byte intermingling instruction, each of the first and second source operands comprising an ordered plurality of fields; and

writing, into a most significant portion of a destination operand, a most significant plurality of fields selected from the first source operand and writing, into a least

significant portion of the destination operand, a least significant plurality of fields selected from the second source operand.

18 (new). The digital system of Claim 1, wherein the byte intermingling circuitry is operable to place most significant bytes of a plurality of fields selected from the second operand into the least significant portion of the destination operand and to place most significant bytes of a plurality of fields selected from the first operand into the most significant portion of the destination operand.

19 (new). The digital system of Claim 1, wherein the byte intermingling circuitry is operable to place least significant bytes of a plurality of fields selected from the second operand into the least significant portion of the destination operand and to place least significant bytes of a plurality of fields selected from the first operand into the most significant portion of the destination operand.